CS 250 Fall 2017 Homework 09 SOLUTION & Grading Guide

Due 11:58pm Thursday, Nov. 9, 2017

Submit your typewritten file in PDF format to Blackboard

1. Text exercise 10.2

Underlying Technology and Organization

1. Text exercise 10.10

Register are highly linked to most pipeline stages. We need to track their lifetime, and forward results back to previous stages. It's expensive on area, which ultimately means it's expensive on power, price and performance after a certain point. Registers take up instruction encoding space. 16 registers take up 4 bits for source and destination, and another 4 if you have 3-operand instructions (e.g. ARM). Therefore, designers create processors with so few registers.

1. Text exercise 11.1

Smartphones use DRAM because SRAM takes a lot of space on chip to store the same amount of data. Also, SRAM has higher manufacturing cost.

1. Text exercise 11.3

Offset within word = 9\*8modulo 64.

For 27th byte, word address = 8\*27/64.

Offset within word = 27\* 8 modulo 64

For 21th byte, word address = 8\*31/64

Offset within the word = 31\*8 modulo 64

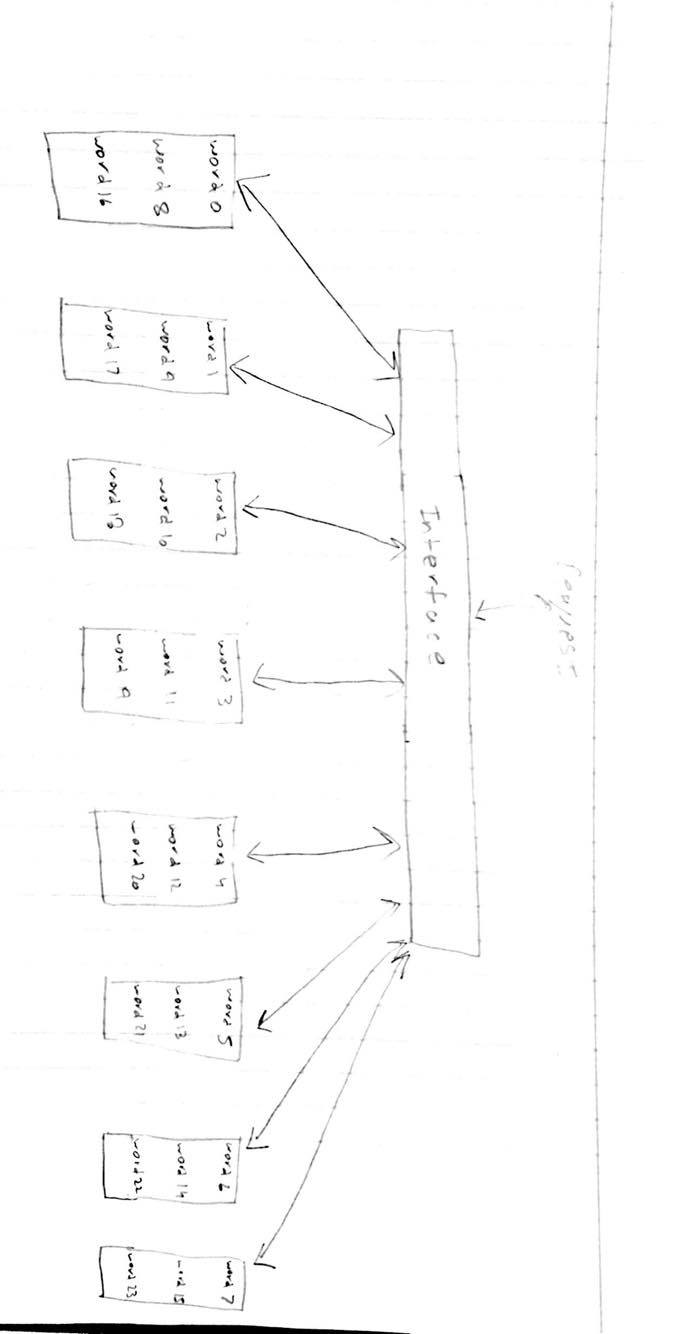
For 120, word address = 8\*120/64

Offset within the word = 120\*8 modulo 64

1. Text exercise 11.5

Alignment fault

1. Text exercise 11.10 including labels for words 0 through 15.



1. Text exercise 12.2

0.804μs

1. Text exercise 12.3, assuming L1 block size is 4 words.

Switch I and j

1. Main memory is byte addressed using 32 bit addresses. The index and offset fields for a direct-mapped, write-back cache design are 11 bits and 5 bits, respectively.
   1. How many bytes of the 32-bit address space can be mapped into this cache?

2^16 bytes

* 1. How many bytes of overhead storage are needed to manage cache access for this cache design?

4096 bytes

* 1. What percentage of all the locations in the cache that store a bit are used to hold memory hierarchy content?

94.12%